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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,365	08/15/2001	Masahiro Takeuchi	15.45/6059	3437

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KONRAD RAYNES VICTOR & MANN, LLP
315 SOUTH BEVERLY DRIVE
SUITE 210
BEVERLY HILLS, CA 90212

EXAMINER	
VU, QUANG D	
ART UNIT	**PAPER NUMBER**
2811	6

DATE MAILED: 06/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,365	TAKEUCHI, MASAHIRO	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-26, drawn to method for manufacturing a semiconductor device, classified in class 438, subclass 221.

II. Claims 27-31, drawn to semiconductor device, classified in class 257, subclass 357.

During a telephone conversation with Alan Raynes on 05/30/2002 a provisional election was made without traverse to prosecute the invention of group I, claims 1-26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 27-31 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,087,243 to Wang.

Regarding claim 19, Wang teaches a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

forming a first layer (11) on a semiconductor substrate;

forming a polishing stopper layer (13) above the first layer;

forming at least one trench (14) by etching the first layer while using the polishing stopper layer as a mask;

forming a dielectric layer (16) in and above the trench; and

planarizing the dielectric layer using the polishing stopper layer (13) as a stopper (see figures 1a-c; column 6, lines 44-50).

Regarding claim 20, Wang teaches the first layer (11) comprises an epitaxial growth layer (see figures 1a-f; column 6, lines 14-18).

Regarding claim 21, Wang teaches removing the polishing stopper layer (13) after planarizing the dielectric layer (see figures 1a-d; column 6, lines 44-54).

Regarding claim 22, Wang teaches an oxidizing at least a portion of the first layer in the at least one trench prior to forming the dielectric layer in and above the trench (see figures 1a-b; column 6, lines 44-48).

Regarding claim 23, Wang teaches forming a pad layer (12) between the first layer (11) and the polishing stopper layer (13) (see figure 1a-c).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,165,854 to Wu.

Regarding claim 1, Wu teaches a method for manufacturing a semiconductor device having a trench isolation region, the method comprising the steps of:

forming a trench (8) in a semiconductor layer;

forming a dielectric layer (14) that fills the trench; and

conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures about 800° C to 1100° C, which overlaps the temperature range of the claimed invention (see figures 1-6; column 4, lines 33-38).

Regarding claim 2, Wu does not explicitly teach the dielectric layer is formed with a film density of at lest 2.1 g/cm^3. The dielectric layer formed by Wu would have inherently had the same density as that of the claimed invention since it is formed by the same method at a temperature that lies within the range disclosed.

Regarding claim 3, Wu teaches a method wherein the temperature of the thermal treatment is about 800° C to 1100° C, which overlaps the temperature range of the claimed invention (column 4, lines 33-38).

Regarding claim 4, Wu teaches a method wherein the temperature of the thermal treatment is about 800° C to 1100° C, which overlaps the temperature range of the claimed invention (column 4, lines 33-38).

Regarding claim 5, Wu teach the dielectric layer is formed using high density plasma chemical vapor deposition (column 4, lines 26-38).

Regarding claim 6, Wu does not explicitly teach forming a well in the semiconductor layer, and conducting a thermal treatment before forming a well. Wu teaches a trench isolation structure (column 4, lines 26-38) used with a CMOS device (column 5, lines 1-15). The CMOS device taught by Wu would have inherently had a well in the semiconductor layer since a CMOS must have at least one well. Wu does not teach forming a well after the conducting a thermal treatment. The order of forming the well and conducting a thermal treatment is seen as a matter of obvious design choice.

Regarding claim 7, Wu teaches a method, wherein the trench includes sidewall surfaces and a bottom surface and a thermally oxidized dielectric layer in the trench (column 4, lines 9-12).

Regarding claims 8 and 9, Wu teaches the temperature of the thermal treatment the sidewall surfaces and the bottom surface of the trench about 800° C to 1100° C, which overlaps the temperature range of the claimed invention (column 4, lines 9-12).

Regarding claim 10, Wu does not teach the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10nm to 100nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal thickness of the oxidation layer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

5. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,165,854 to Wu as applied to claim 1 above, and further in view of US Patent No. 6,087,243 to Wang.

Regarding claim 11, Wu does not teach the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate. However, Wang teaches the semiconductor layer (11) comprises an epitaxial growth layer formed on a semiconductor substrate (column 6, lines 14-18). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wang into the method taught by Wu since it is desirable to provide high quality silicon to form devices in.

Regarding claim 12, Wu does not teach the epitaxial growth layer has a thickness of at least 2 micrometer. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal thickness of the epitaxial layer, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Regarding claim 13, Wu does not teach the trench is formed with a trench width of no greater than 0.35 micrometer. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal width of the trench, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

6. Claims 14-18 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,087,243 to Wang.

Regarding claim 14, Wang teaches a method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a trench (14) in a semiconductor layer;

forming a dielectric layer (16) in the trench; and

heating the dielectric layer at a temperature about 900° C to 1100°, which overlaps the temperature range of the claimed invention (see figures 1a-h; column 6, lines 44-60).

Regarding claim 15, Wang teaches forming a trench oxide layer (15) on the sidewalls and bottom of the trench prior to forming the dielectric layer in the trench (see figure 1b; column 6, lines 44 - 47).

Regarding claim 17, Wang teaches heating the dielectric layer at a temperature of 900 ° C to 1100 ° C, which overlaps the temperature range of claimed invention. Wang does not teach heating the dielectric layer is carried out for a time in the range of 20 minutes to 120 minutes. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal time of annealing, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Regarding claim 18, Wang teaches forming at least one transistor adjacent to the trench isolation region (see figure 1H; column 7, lines 23 - 34), the at least one transistor being formed after heating the dielectric layer at a temperature of 900 ° C to 1100 ° C, which overlaps the temperature range of the claimed invention.

Regarding claim 24, Wang teaches subjecting the dielectric layer to a thermal treatment at a temperature about 900° C to 1100° C after removing the polishing stopper layer, which overlaps the temperature range of the claimed invention (column 6, lines 44 – 60).

Regarding claim 25, Wang does not teach the thermal treatment is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to find the optimal concentration of oxygen in the atmosphere, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Regarding claim 26, Wang does not teach the dielectric layer is formed using high density plasma chemical vapor deposition. It would have been to one having ordinary skill in the art to select HDPCVD as a matter of obvious design choice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QVU
June 14, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800